

What is claimed is:

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1. A method of operation of a delay lock loop comprising:
comparing a phase of a first clock signal with a phase of a second clock signal to
generate a first control signal;
delaying the first clock signal to generate a first delayed clock signal;
comparing a phase of the first delayed clock signal with the phase of the second
clock signal to generate a second control signal; and
10 shifting a phase of the first clock signal in response to the first control signal and
the second control signal.
 2. The method of claim 1 wherein shifting comprises:
responsive to the first control signal, shifting the phase of the first clock signal
15 by a first amount; and
responsive to the second control signal, shifting the phase of the first clock
signal by a second amount, wherein the second amount is greater than the first amount.
 3. The method of claim 1 further comprising:
20 delaying the second clock signal to generate a second delayed clock signal;
comparing a phase of the second delayed clock signal with the phase of the first
clock signal; and
shifting the phase of the first clock signal a third amount in response to the third
control signal.
 - 25 4. The method of claim 3 wherein the third amount is substantially equal to the
second amount.

5. A method of setting a delay value in a delay lock loop comprising:
delaying a first signal in a variable delay line to generate a second signal;
comparing a phase of the first signal with a phase of the second signal to
5 generate a first control signal;
delaying the first signal by a first substantially fixed amount to generate a third
signal;
comparing the phase of the second signal with a phase of the third signal to
generate a second control signal;
10 responsive to the first control signal, adjusting the variable delay line by a first
delay amount; and
responsive to the second control signal, adjusting the variable delay line by a
second delay amount, the second delay amount being greater than the first delay
amount.
- 15 6. The method of claim 5 further comprising:
delaying the second signal by a second substantially fixed amount to generate a
fourth signal;
comparing the phase of the first signal with a phase of the fourth signal to
20 generate a third control signal; and
responsive to the third control signal, adjusting the variable delay line by a third
delay amount.
7. The method of claim 6 wherein the second delay amount and the third delay
25 amount are substantially equal.
8. The method of claim 6 wherein the first substantially fixed amount and the
second substantially fixed amount are substantially equal.

9. The method of claim 6 wherein the first delay amount and the second delay amount are opposite in polarity.

10. A method of aligning the phase of a first signal external to a device and the
5 phase of a second signal internal to the device comprising:
receiving the first signal into the device, and subjecting the first signal to a device boundary delay to produce an internal first signal;
delaying the internal first signal in a variable delay line to generate the second
signal, the variable delay line having a fine adjustment control and a coarse adjustment
10 control;
delaying the second signal a substantially fixed amount to produce a delayed second signal;
comparing the internal first signal with the second signal, and responsive thereto, driving the fine adjustment control; and
15 comparing the internal first signal with the delayed second signal, and responsive thereto, driving the coarse adjustment control.

11. The method of claim 10 wherein prior to delaying the second signal or comparing the internal first signal with the second signal, the method further comprises
20 subjecting the second signal to an additional delay substantially equal to the device boundary delay.

12. The method of claim 10 wherein the variable delay line has a second coarse adjustment control and the method further comprises:
25 delaying the internal first signal the substantially fixed amount to produce a delayed internal first signal; and
comparing the delayed internal first signal and the second signal, and responsive thereto, driving the second coarse adjustment.

13. The method of claim 12 wherein the first coarse adjustment and the second coarse adjustment result in adjustments of opposite polarity.

14. In a memory device having data output drivers configured to drive data signals external to the memory device, a method of aligning the data signals with an external clock signal comprising:

receiving the external clock signal;

delaying the external clock signal in a variable delay line having a variable delay associated therewith, to produce an internal clock signal;

generating a phase difference between the external clock signal and the internal clock signal;

comparing the phase difference to a threshold;

when the phase difference is above the threshold, changing the variable delay a first delay amount;

when the phase difference is not above the threshold, changing the variable delay a second delay amount, the second delay amount being less than the first delay amount; and

driving a control input of the data output drivers with the internal clock.

15. The method of claim 14 wherein the data output drivers are sequential devices having clock inputs, and driving a control input comprises driving the clock inputs of the sequential devices.

16. The method of claim 14 wherein the data output drivers are devices having output enable inputs, and driving a control input comprises driving the output enable inputs of the data output drivers.

17. The method of claim 14 wherein generating a phase difference and comparing the phase difference comprise:

5 delaying the internal clock signal by an amount substantially equal to the threshold to generate a delayed internal clock signal; and
 comparing the delayed internal clock signal to the external clock signal.

18. The method of claim 14 wherein generating a phase difference and comparing the phase difference comprise:

10 delaying the external clock signal by an amount substantially equal to the threshold to generate a delayed external clock signal; and
 comparing the delayed external clock signal to the internal clock signal.

19. The method of claim 14 wherein the external clock signal has a period
15 associated therewith, and the variable delay line delays the external clock signal such that the internal clock signal lags the external clock signal by an integer number of periods.

20. In a delay line having a variable delay, a method of changing the variable delay
20 comprising:

 comparing a phase of a signal input to the delay line with a phase of a signal output from the delay line to produce a phase difference;

 when the phase difference is larger than a first threshold, adjusting the variable delay by a first delay amount; and

25 when the phase difference is not larger than the first threshold and is larger than a second threshold, adjusting the variable delay by a second delay amount, the second delay amount being less than the first delay amount.

21. The method of claim 20 further comprising:
responsive to the comparing, when the phase difference is smaller than the
second threshold, holding the variable delay constant.
- 5 22. The method of claim 20 wherein the delay line comprises a plurality of delay
elements, each of the plurality of delay elements having a unit delay, and wherein the
second delay amount is substantially equal to one unit delay.
- 10 23. The method of claim 22 wherein the first delay amount is substantially equal to
an integer number of unit delays.
24. A phase detector comprising:
a first input node, a second input node, a first output node, and a second output
15 node;
a first phase comparator coupled between the first input node, the second input
node, and the first output node;
a first delay line coupled to the first input node; and
a second phase comparator coupled between the first delay line, the second input
20 node, and the second output node.
25. The phase detector of claim 24 further comprising:
a third output node;
a second delay line coupled to the second input node; and
25 a third phase comparator coupled between the first input node, the second delay
line, and the third output node.

26. The phase detector of claim 24 wherein the first phase comparator is configured to produce at least one fine delay line adjustment control, and the second phase comparator is configured to produce at least one coarse delay line adjustment control.

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27. A delay lock loop comprising:

a variable delay line including a plurality of delay cells;

a shift register having a plurality of storage elements, each of the plurality of storage elements corresponding to one of the plurality of delay cells, the plurality of storage elements being arranged in a plurality of blocks of storage elements, the shift
10 register having a fine control input node, and a coarse control input node; and

a phase detector having a fine adjustment output node coupled to the fine control input node, and having a coarse adjustment output node coupled to the coarse control input node.

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28. The delay lock loop of claim 27 wherein the shift register is configured to shift one of the plurality of storage elements in response to an asserted signal on the fine control input node.

20 29. The delay lock loop of claim 27 wherein the shift register is configured to shift one of the plurality of blocks of storage elements in response to an asserted signal on the coarse control input node, such that the variable delay line changes by more than one of the plurality of delay cells in response to the asserted signal.

25 30. The delay lock loop of claim 27 wherein the variable delay line includes an input node and an output node, and wherein the phase detector is configured to measure a phase difference between a signal on the input node of the variable delay line and a signal on the output node of the variable delay line.

31. The delay lock loop of claim 30 wherein the phase detector is configured to assert a coarse control signal on the coarse adjustment output node when the phase difference is above a threshold, and to assert a fine control signal on the fine adjustment output node when the phase difference is below the threshold.

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32. The delay lock loop of claim 27 wherein the plurality of delay cells each exhibit substantially the same delay.

33. The delay lock loop of claim 27 wherein the plurality of delay cells do not all
10 exhibit the same delay.

34. A variable delay line comprising:
a coarse adjustment portion comprising a first plurality of delay cells and a first shift register; and

15 a fine adjustment portion comprising a second plurality of delay cells and a second shift register, wherein each of the first plurality of delay cells has a delay value larger than that of each of the second plurality of delay cells.

35. The variable delay line of claim 34 wherein the first shift register is configured
20 to be responsive to coarse adjustment signals from a phase detector.

36. The variable delay line of claim 34 wherein the second shift register is configured to be responsive to fine adjustment signals from a phase detector.

37. An integrated circuit comprising:
a variable delay line having an input node, an output node, a fine adjustment input node, and a coarse adjustment input node; and
5 a phase detector configured to compare a signal on the input node with a signal on the output node and drive signals onto the fine adjustment input node and the coarse adjustment input node.
38. The integrated circuit of claim 37 wherein the fine adjustment input node
10 comprises:
a fine increase adjustment input node; and
a fine decrease adjustment input node.
39. The integrated circuit of claim 37 wherein the coarse adjustment input node
15 comprises:
a coarse increase adjustment input node; and
a coarse decrease adjustment input node.
40. The integrated circuit of claim 37 further comprising an output driver responsive
20 to the signal on the output node of the variable delay line.
41. The integrated circuit of claim 37 wherein the output driver is a synchronous element having a clock input node, and the clock input node is coupled to the output node of the variable delay line.
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42. The integrated circuit of claim 37 wherein the output driver includes an output enable input node coupled to the output node of the variable delay line.
43. The integrated circuit of claim 37 wherein the integrated circuit is a memory
30 device.

44. The integrated circuit of claim 37 wherein the integrated circuit is an application specific integrated circuit.

45. The integrated circuit of claim 37 wherein the integrated circuit is a processor.

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46. A processing system comprising:

a processor; and

a memory having a delay lock loop comprising:

a variable delay line including a plurality of delay cells;

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a shift register having a plurality of storage elements, each of the plurality of storage elements corresponding to one of the plurality of delay cells, the plurality of storage elements being arranged in a plurality of blocks of storage elements, the shift register having a fine control input node, and a course control input node; and

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a phase detector having a fine adjustment output node coupled to the fine control input node, and having a coarse adjustment output node coupled to the coarse control input node.

47. The processing system of claim 46 wherein the shift register is configured to shift one of the plurality of blocks of storage elements in response to an asserted signal on the coarse control input node, such that the variable delay line changes by more than one of the plurality of delay cells in response to the asserted signal.

48. The processing system of claim 46 wherein the variable delay line includes an input node and an output node, and wherein the phase detector is configured to measure a phase difference between a signal on the input node of the variable delay line and a signal on the output node of the variable delay line.

49. A processing system comprising:
a processor; and

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a memory having a delay lock loop that includes a phase detector comprising:

a first input node, a second input node, a first output node, and a second output node;

a first phase comparator coupled between the first input node, the second input node, and the first output node;

a first delay line coupled to the first input node; and

a second phase comparator coupled between the first delay line, the second input node, and the second output node.

50. The processing system of claim 49 wherein the phase detector further comprises:

a third output node;

a second delay line coupled to the second input node; and

a third phase comparator coupled between the first input node, the second delay line, and the third output node.

51. A processing system comprising:

a processor; and

a memory having a delay lock loop that includes a variable delay line comprising:

a coarse adjustment portion comprising a first plurality of delay cells and a first shift register; and

a fine adjustment portion comprising a second plurality of delay cells and a second shift register, wherein each of the first plurality of delay cells has a delay value larger than that of each of the second plurality of delay cells.

52. The processing system of claim 51 wherein the first shift register is configured to be responsive to coarse adjustment signals from a phase detector.

53. The processing system of claim 52 wherein the second shift register is

configured to be responsive to fine adjustment signals from a phase detector.